

Crystallographic Modification of Hard mask Properties

Abstract

A hardmask layer in the back end of an integrated circuit is formed from TaN having a composition of less than 50% Ta and a resistivity greater than 400 $\mu\text{Ohm-cm}$, so that it is substantially transparent in the visible and permits visual alignment of upper and lower alignment marks through the hardmask and intervening layer(s) of ILD. A preferred method of formation of the hardmask is by sputter deposition of Ta in an ambient containing N_2 and a flow rate such that $(\text{N}_2 \text{ flow})/(\text{N}_2 + \text{carrier flow}) > 0.5$.